fortémedia

FM23-382
Mixed-signal Voice Processor
for Mobile Applications

Product Data Sheet
(Product Information) version 1.0

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Status Information

The status of this Product Data Sheet is **Product Information**.

Advance Information

Information for designers concerning Fortemedia product in development. All values specified in the document are the target values of the design. Minimum and maximum values, if specified, are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by Fortemedia without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalized. All values specified in the document are the target values of the design. Minimum and maximum values, if specified, are only given as guidance to the final specification limits and must not be considered as the final values.

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Product Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Product Data Sheets supersede all previous document versions.

Note

While every case has been taken to ensure the accuracy of the contents in this Data Sheet, Fortemedia cannot accept responsibility for any errors. Fortemedia reserves the right to make technical changes to its products as part of its development program.

FIGURES

TABLES

Document History

Revision	Date	Description
V0.1	Oct 30, 2012	Initial
V0.2	Dec 27, 2012	Modify the CSP pin definition, add QFN package pin description
V0.3	Jan 29, 2013	Change PDMDATA & PDMCLK pin to Reserved pin
V0.4	Feb 20, 2013	Modify MCLK and V_{IH},V_{IL},V_{OH} and V_{OL} based on the standard, Change the minimum of VDD and VDDA from 1.62V to 1.71 V
V0.5	Mar 2, 2013	Change 3.3V voltage tolerance for all digital inputs, Add VDD ripple 100mV in Table 5
V0.6	Mar 11, 2013	Editorial updates, for 1st release
V0.7	May 03,2013	Update Order Code & Package Dimension for FM23-CE-382B
V1.0	Aug 30,2013	Editorial updates, for official release

1. Introduction

Fortemedia FM23 is a low-cost, ultra-compact, mixed-signal voice processor that integrates advanced acoustic echo cancellation (AEC) and beamforming noise reduction capabilities targeted for easy integration into mobile device applications.

With Fortémedia's proprietary voice processing technology, the FM23 uses advanced beam-forming technology and filters out the unwanted background noises, and the AEC eliminates any acoustic echo in handheld and handsfree voice conversation, providing natural and clear full-duplex conversations for users in any environment.

1.1 Overview

With integrated Analog-to-Digital(A/D) and Digital-to-Analog(D/A) interfaces on chip, the FM23 is a mixed signal voice processor integrating an on-chip digital signal processor (DSP) and hardware computation accerlerator with its RAM, ROM, and Serial Host Interface. The FM23 is packaged in a 20-pin WLCSP and occupies a footprint of 2.6 x 2.2 mm^2 such that minimal board space is taken up.

1.2 Key Features

- **Highly integrated mixed-signal Voice PRocessor**

  - Low-cost, and high performance voice processor with built-in hardware support for analog signal input and output
  - Three 16-bit differential ADC's for two microphone inputs and one line level input, each sampling at 8KHz at 84 dB SNR
  - Each analog microphone input channel has built-in Programmable Gain Adjust(PGA) and pre-amplifier
  - One 16-bit differential DAC for the line level output
  - No external RAM required
  - Serial Host Interface(SHI) is I^{2}C-compatible and supports on-the-fly command and parameter download for processor control and configuration, at speed up to 400Kbps
  - Flexible clocking input with built-in Phase-Locked Loop (PLL)
    - supports 3 to 32MHz in 1 MHz steps, and
    - 4.096 to 40.96 MHz with a multiple of 4.096MHz steps
  - Low power consumption:
    - 1-microphone or 2-microphone mode: ~25mW.
    - Power down mode: current consumption of 5µA(typical)
    - 1.8V for all analog power domain
    - 1.8V for digital and core power domain.

- **Specifications**
  - 0.11um low power process
  - Packages:
    - Package: 20-ball WLCSP, 2.6 x 2.2 mm^2, 0.5mm pitch

FM-23 Voice Processing Capability	Inbound Voice from far-end	Outbound Voice towards far-end
Acoustic Echo Canceller		Yes
User Configurable 1- and 2- microphone Voice Processing		Yes
Stationary and Non-Stationary Noise Reduction		Yes
Beamforming		Yes
Automatic Gain Control	Yes	Yes
Audio Equalization	Yes	Yes
Dynamic Range Control	Yes	Yes
Analog signal input and output	Yes	Yes

Summary of FM-23 Voice Processing Functions

1.3 Pin Configuration
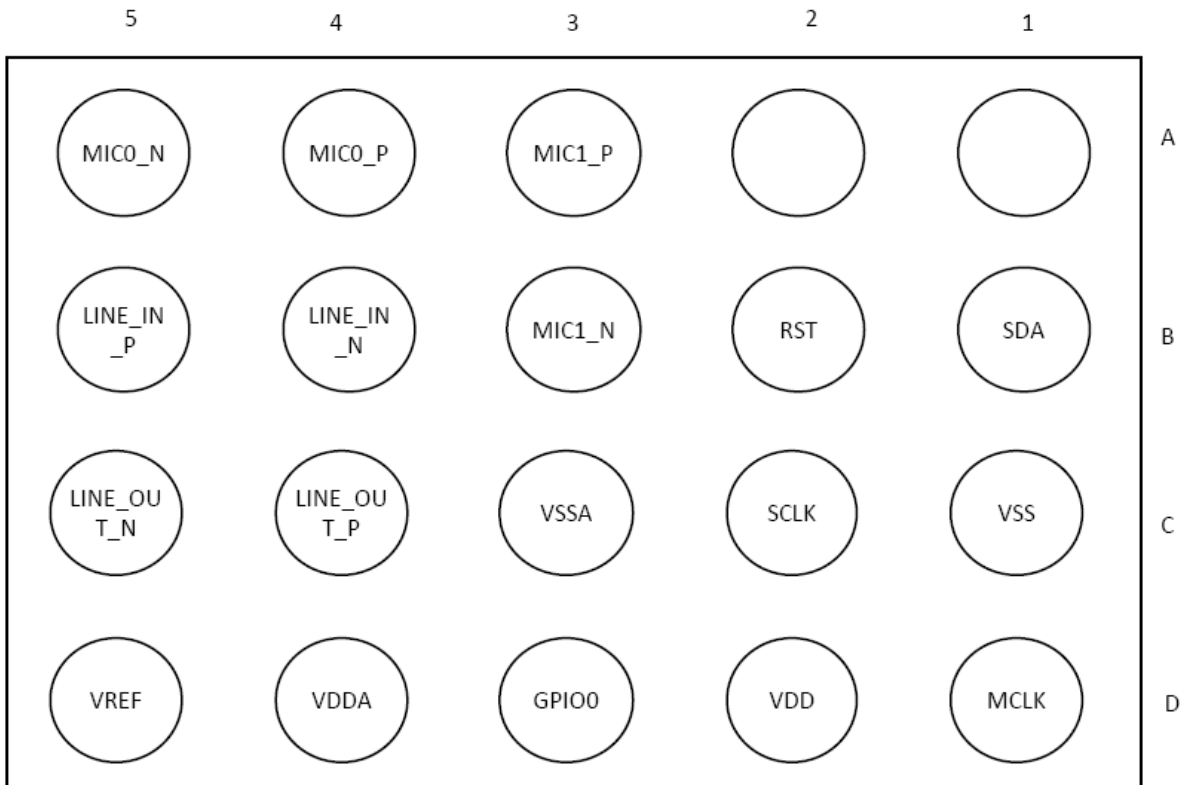
Figure 1: 20-pin WLCSP Pin Configuration - Bottom View

1.4 Device Terminal Functions

Clock	Lead	Pad Type	Supply Domain	Description
MCLK	D1	In	VDD	For external clock in

Controls	Lead	Pad Type	Supply Domain	Description
GPIO0	D3	In/Out	VDD	General Purpose Input/Output
RST_	B2	In	VDD	Reset control, active high

Power Supplies	Lead	Description
VDD	D2	Positive supply for digital input/output
VDDA	D4	Positive supply for analog
VSSA	C5	Ground Connection – Analog Ground
VSS	C1	Ground Connection – Digital Ground
VREF	VREF	Reference Voltage Output – about ½ of VDDA

Serial Host Interface (SHI)	Lead	Pad Type	Supply Domain	Description
SDA	B1	In/Out	VDD	IIC-compatible serial slave data
SCL	C2	In	VDD	IIC-compatible serial slave clock

| Analog Audio I/O	Lead	Pad Type	Supply Domain	Description
MIC0_P	A4	Analog In	VDDA	main microphone input
MIC0_N	A5	Analog In	VDDA	main microphone input
MIC1_P	A3	Analog In	VDDA	secondary microphone input
MIC1_N	B3	Analog In	VDDA	secondary microphone input
LINE_IN_P	B5	Analog In	VDDA	line input
LINE_IN_N	B4	Analog In	VDDA	line input
LINE_OUT_P	C4	Analog Out	VDDA	line output
LINE_OUT_N	C5	Analog Out	VDDA	line output

1.5 Internal Hardware Block Diagram
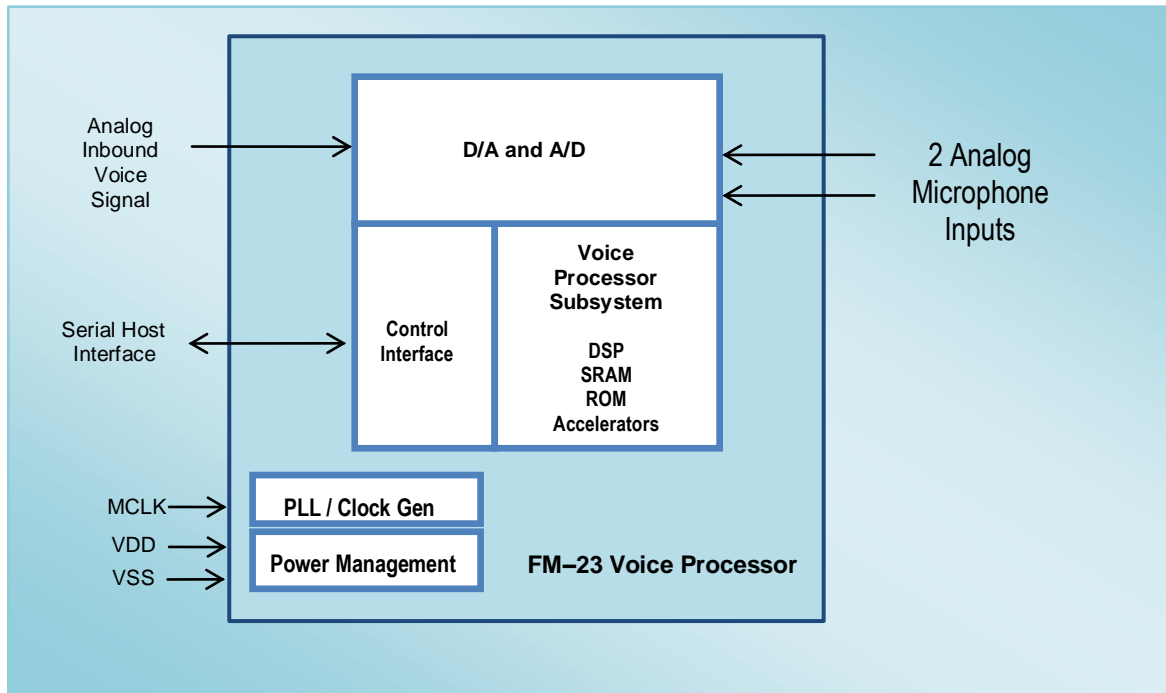
Figure 2: FM23 Hardware Block Diagram

1.6 System Application Block Diagram
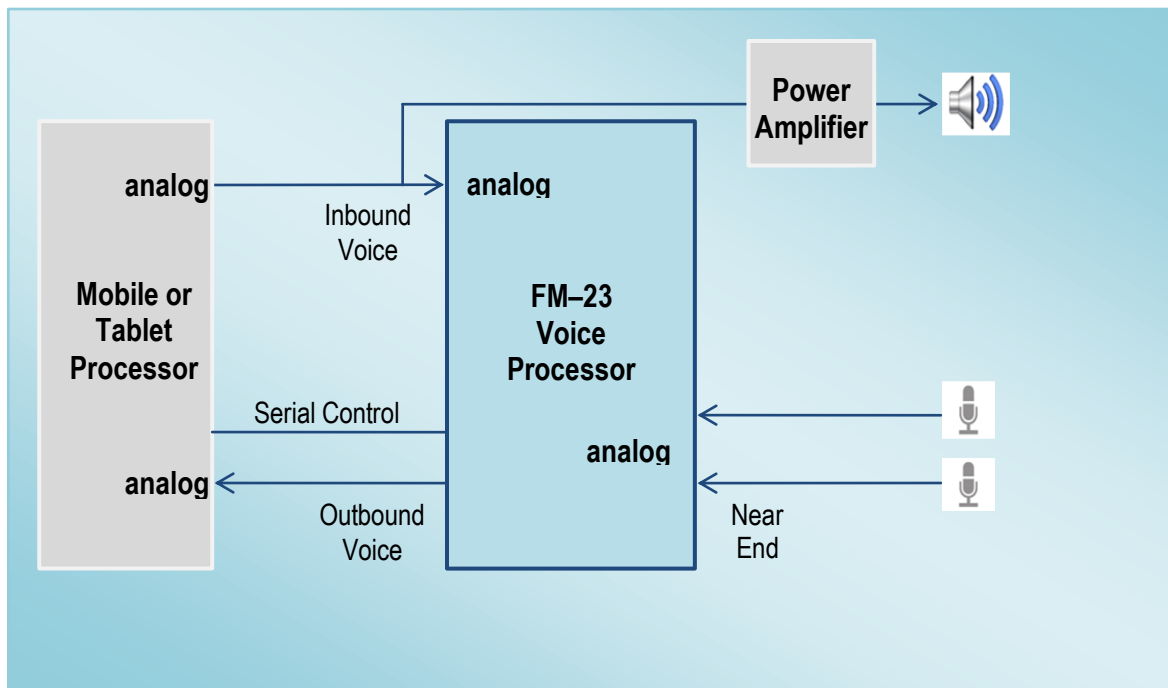
Figure 3: FM23 Example Usage: with Mobile Processor

2. Functional Description

2.1 Serial Host Interface - SHI (Pins B1, C2)

The FM23 implements a Serial Host Interface (SHI) which is an IIC-compatible, slave mode only, serial interface between FM23 and an external processor for control information communications.   It can be used to

- Transmit and receive control commands at run-time, and
- Download the necessary initialization configuration parameters during reset and power-up, should the system designer elect this option.

On this SHI, FM23 communicates to the host processor through a bi-directional serial data line (SDA) and a serial clock line (SCL). The FM36 SHI operates as a slave device and its serial clock is driven from the host. The master on the host processor controls SCL clocking, data transfer start bit and stop bit, and also addressing of slave devices.   The FM23 supports 8-bit address and its device address is "**0xC0**".

Depending on the host processor instruction, the SHI can operate as a transmitter (writing data) or a receiver (reading data). Note that the SHI interface supports the standard clock speed of 100 kHz or up to a maximum speed of 400 kHz (if MCLK is above 10MHz).

The standard byte format of SHI data line must be 8–bit long in every byte. Each byte consists of 8 bits plus 1 acknowledge bit, and it is one data bit per clock pulse. If operating as a receiver, it will return an acknowledge bit upon each successful byte transfer, otherwise it will return a NOACK signal. There is no restriction on the maximum number of bytes per data transfer. Data transfer can be aborted if the master device generate a STOP condition to terminate a transfer. Each data transfer frame must start with a START or a RESTART symbol and ends by a STOP symbol.

Table 1: SHI START and STOP data transition

S: START	SDA transition from 1 to 0 when SCL=1
P: STOP	SDA transition from 0 to 1 when SCL=1

Within the data transfer frame, multiple command sequences are allowed and there is no restriction on the maximum numbers of bytes per frame. Each command sequence starts with a sync word "0xFCF3", follows by a command entry byte (e.g. 0x3B is MEM_WRITE) and number of bytes per specific command. The following figures and tables summarize the details for the SHI command sequence.

Figure 4: SHI Data Transfer Command Protocol

Figure 5: SHI Command Sequence

Table 2: SHI Command Name

Command Entry Name	Command Entry Byte	Number of the bytes for each functional bytes		
		Address Byte	Data Byte	Total (cmd+address+data)
MEM_WRITE	0x3B	2	2	5
MEM_READ	0x37	2	0	3
REG_READ	0x60	1	0	2

Table 3: SHI Command Byte Format

Serial Command Entry Byte								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Description	Access object type				Read /Write	Data byte number		Address byte number
Value Details	Data Memory (0011b) DataPort(0110b)(e.g. register)				Read: 0 Write: 1	2bytes (01b) 1byte (00b) 0byte (11b)		Two address bytes(1b) Data memory access One address byte(0b) Data port access

Table 4: SHI Command Byte Bit Definition

| Data length		1byte
Bit	Pattern	Descriptions
D7 - D4	0011b	For accessing Data Memory
	0110b	For reading the Data ports.
D3	0b	Read
	1b	Write
D2-D1	00b	1 byte data write, or in Data Port Read mode.
	01b	2 bytes data write
	11b	0 byte data (in Data Memory Read mode).
D0	1b	Two address bytes for accessing Data Memory
	0b	One address byte for reading Data Port (Either 0x25 for lower byte or 0x26 for upper byte.

2.2 Analog Data Input (A4, A5, A3, B3, B4, B5)

The FM23 has three ADC's that are sigma-delta converters with 16-bit resolution and sampling at 8 kHz. All 3 converters are of differential analog input type, and each of the microphone inputs (MIC0 and MIC1) has built-in microphone pre-amplifiers. The line-in (LINE_IN) analog input contains is used in FM23-382 for the echo reference input when echo cancellation function is applied. It is connected to the line-out or speaker-out ports from the output of the audio codec system.

The differential inputs of MIC0/1 ADCs are 0.56 Vpp in full scale. Gain range is from 0 to 21dB in +3 dB increments programmable by setting the PGA gain.

The differential input of Line in ADC is 2.0 V_{PP} in full scale. Gain range is from -3 to +9dB in +3 dB increments programmable by setting the PGA gain.

For details on programming the attenuation and gains of ADCs, please refer to the "FM23-382 Configuration Guide" document.
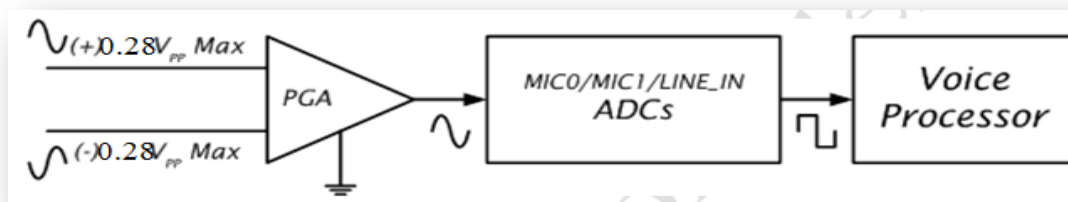
Figure 6: Analog Mic0/Mic1 Input Block Diagram
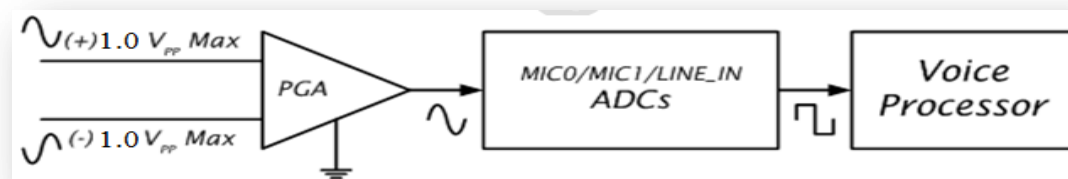
Figure 7: Analog Line-In Input Block Diagram

A brief summary of recommended Microphone Specification for the analog microphones is tabulated below:

Parameter	Value
Type	Electric Condenser Microphone, Omni-directional
Sensitivity	-42dB±3dB (1V/Pascal)
Operating Voltage	2V (standard)
Impedance	2.2kΩ maximum

2.3 Analog Data Output (C4, C5)

The FM23-382 has a Digital-to-Analog Converter (DAC) working at 8 kHz sample rate. There are 16 bits thermometer code input to DAC and DAC provides differential analog output with programmable attenuations and gains.

The LINE_OUT DAC provides an analog voice output signal and sends the processed voice signal to the uplink voice path of the system.   The differential input of Line Output DAC is 2.0 V_{PP} in full scale.

The DAC programmable gain control table is listed on Table 5 as the following. The 3-bit setting controls DAC from 0dB to -21 dB with a -3 dB increment.

For details on programming the attenuation and gains of ADCs, please refer to the "FM23-382 Configuration Guide" document.
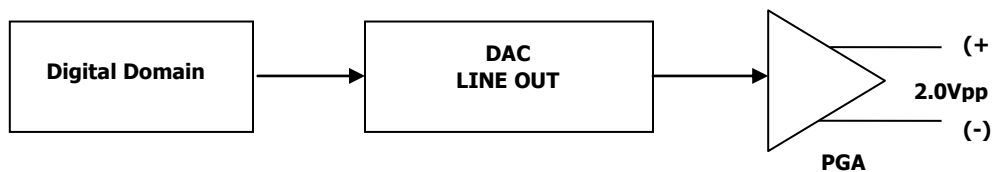
Figure 8: Analog Output Block Diagram

2.4 Power

The FM23-382 has two power domains, the digital with a V_{DD} pin, and analog with a V_{DDA} pin. The analog domain supplies all the analog circuitry and the on-chip PLL. The domain supplies to the DSP and I/O's.

For better immunity of noise, the user should separate the analog and digital planes in the system board design with proper ferrite beads or resistors.

2.5 Clock (D1)

The FM23-382 provides multiple external clocks which can be commonly found in cellular phone platforms. For the external clock input, 3MHz to 32MHz with a multiple of 1MHz or 4.096 MHz to 40.96 MHz with a multiple of 4.096 MHz can be applied.

To set up various input frequency, please refer to parameter "**0x1E50**" in "FM23-382 Parameters Tuning Guide".

The recommended external clock usage is summarized in the table below:

Clock	Recommended Value
Operation frequency	3MHz to 32MHz with a multiple of 1MHz. 4.096 MHz to 40.96 MHz with a multiple of 4.096 MHz.
Frequency tolerance	$\pm$ 100 ppm

2.6 Reset and warm restart

To trigger the internal power-up reset circuit, the voltage of VDD digital power must be lower than 0.4V before ramping high to restart a reset process.

Note that there should be a minimum waiting time, t_{RST} (see table 7), between power-off and power-on. For systems with long power down discharge time, it is recommended to incorporate a discharge circuitry for the power-on restart process.

The RESET_ pin should have a 100kΩ pull-up resistor when this function is not used.

2.7 Power Down Mode

The FM23 supports a power-down mode by the host setting the address 0x1E79 via the serial control interface.   FM23 only supports power down reset mode.

The minimum power-down period would be around 100us, and the power-down mode can be exited and FM-23 resumes operation by applying Reset_ pin.

If the power-down resume mode is not selected, the parameters for the FM23 must be reloaded after recovering from power-off. For more details, please refer to the "FM23-382 Configuration Guide".

2.8 Bypass Mode - Analog Communication Mode

The FM23 supports an analog bypass mode by the host processor setting a register via the serial host control interface, and this mode is often referred to as the Analog Communication mode or Analog Communication bypass.

The analog input signal is routed directly to the analog output signal, bypassing the internal ADC, DSP, and DAC. Note that the gain controls and internal pre-amplifiers are still working with the input and output signal.

In this mode, the gain settings of the programmable PGA are saved and another set of new gains can be set for this analog communication bypass. Upon exit of this Analog Communication Bypass mode and resuming normal operation mode, the saved gains can be restored.

2.9 Normal Operation

The normal operation mode is working when IRQ_ANA pin is at logic low state and triggered by a falling edge.

In the normal operation mode, the FM-23 can be set up to perform voice processing in either single-microphone input mode or dual-microphone input mode, depending on the application's system design and usage.   For both cases the acoustic echo cancellation and stationary noise reduction functions are always present.

For a dual-microphone system, the additional beamforming processing that allows directional sound pick-up should provide additional noise suppression benefits to the user since it is effective in reducing non-stationary background noises.

2.10 Operational States

POWER
OFF

Apply
power

Remove
power

Hardware
RESET

10 ms after
RESET_=high

RESET_=low

Parm(0x1E75)←0

Software
RESET

RESET_=low

Operational

RESET_=low

**Parm(0x1E61,bit12)←1
13ms after RESET_=High**

Power
Down

10 ms after
**Power_down
Parameters
Downloading**

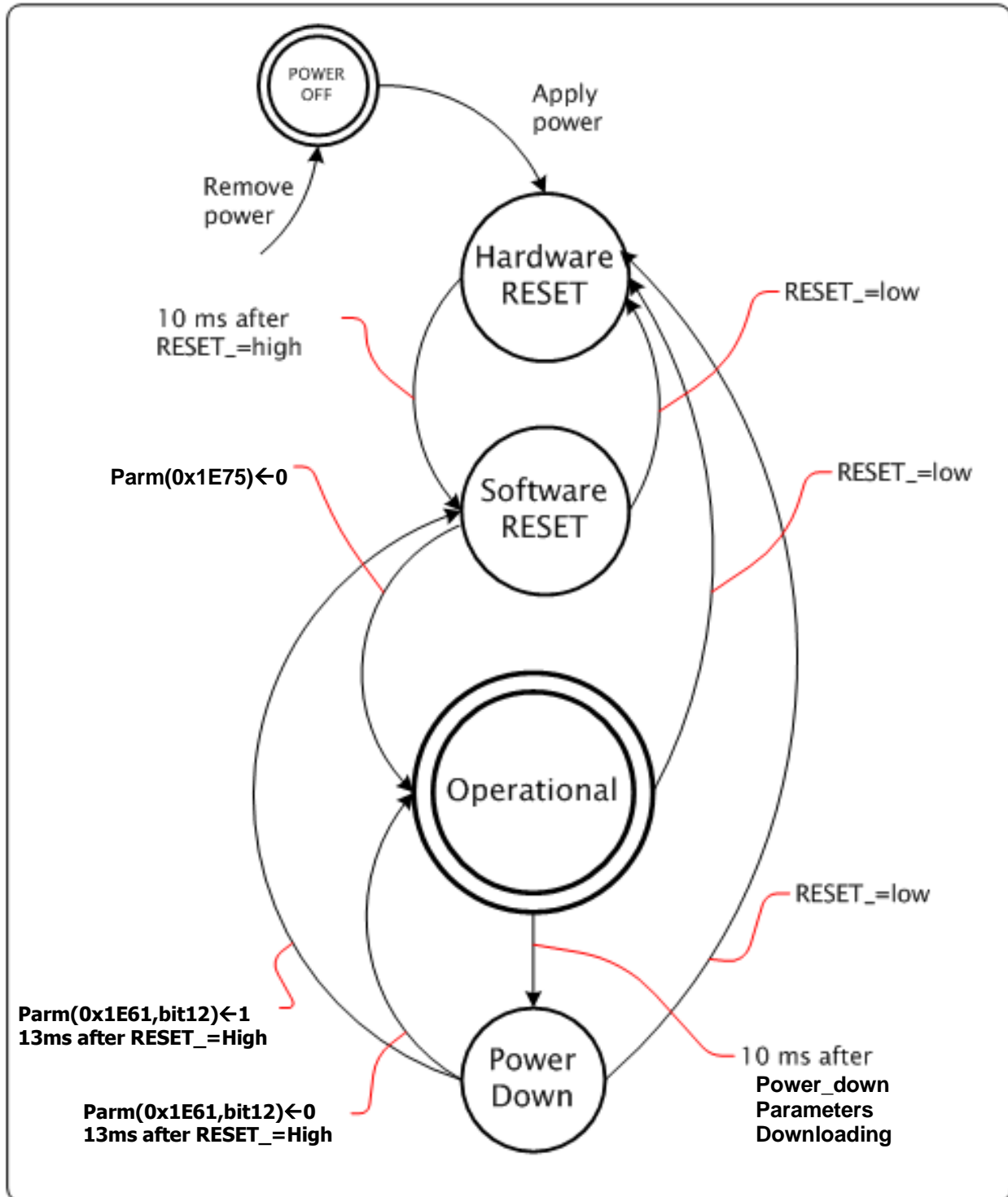**Parm(0x1E61,bit12)←0
13ms after RESET_=High**

Figure 9: Operation State Transition Diagram

3. Electrical and Timing Specification

Note that all data in this section are measured at room temperture and in normal operating condition.

3.1 Absolute Maximum Ratings

Absolute maximum continuous ratings are those values beyond which damage to the device could occur. Exposure to those conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under these conditions is not implied.

Table 5: Absolute Maximum Ratings

Parameter	Symbol	Min	Max Rating	Unit
Digital Power Supply Voltage	VDD	-0.5	2.5	V
Analog Power Supply Voltage	VDDA	-0.5	2.5	V
Latch Up Current	LU	-200	200	mA
Storage Temperature	T_{stg}	-40	150	^0C
Juntion Temperature	T_J	-	125	^0C
ESD (Human body model)	VESDHBM	-2000	2000	V
ESD (Machine model)	VESDMM	-200	200	V

3.2 DC Characteristics

Table 6: DC Characteristics

| Parameters and Symbols		Specification			Unit	Conditions/Remarks
		Min	Typ	Max		
Power Supply for the Digital CORE domain	V_{DD}	1.71	1.8	2.0	V	
Power Supply for the Analog domain	V_{DDA}	1.71	1.8	2.0	V	
Active Power Supply Current	I_{SU}	-	10		mA	In ANA_COM bypass
		-	13		mA	1 microphone mode
		-	13		mA	2 microphones mode
Total Power Dissipation (Based on two microphones)	T_{PD}	-	23		mW	V_{DD}=1.8V, V_{DDA}=1.8V, T_{amb}=25°C
Power Down Current	I_{PD}	-	5		μA	
Input Leakage Current	I_{IH}	-	-	10	μA	V_{DD}=V_{DDA}=1.8V
	I_{IL}	-	-	10	μA	V_{DD}=V_{DDA}=0
Input Voltage High	V_{IH}	0.65VDD	-	VDD+0.3	V	
Input Voltage Low	V_{IL}	-0.3	-	0.35VDD	V	
Output Voltage High	V_{OH}	VDD-0.45	-	-	V	
Output Voltage Low	V_{OL}	-	-	0.45	V	
Input Capacitance	C_{IN}	-	10	-	pF	
VDD Power Ripple (AC element)	-			100	mV	Ripple should be limited for AC performance.

3.3 Timing Characteristics

Table 7: Timing Characteristics

| Parameters and Symbols		Specification			Unit	Conditions/Remarks
		Min	Typ	Max		
Reset Holding Time (low)	t_{RST}	60	-	-	μs	
Power-Down Active Time	T_{PDA}	6.6				
Parameters Restore Time after Reset	t_{PARA}	4	-	-	ms	
Setup time from master clock to rising edge of RST	tCLK2RST	80			us	
LINE_OUT Output Signal Delay Time After Setting Parameters	t_{OUT}	-	TBD	-	ms	see footnote*
Digital Input Raising Time	t_{IR}	-	5	-	ns	C_L=20pF (typ and max) No load (min)
Digital Input Falling Time	t_{IF}	-	5	-	ns	
Digital Output Raising Time	t_{OR}	-	5	-	ns	R_L=1.25kΩ, C_L=20pF (typ and max). No load (min).
Digital Output Falling Time	t_{OF}	-	5	-	ns	
Master Clock Frequency	F_{MCK}	3	-	32	MHz	MCLK pin
		4.096	-	40.96	MHz	
Master Clock Duty Cycle	D_{MCK}	45	50	55	%	MCLK pin
SHI Clock Frequency (SCK)	F_{SCK}	-	100	400	kHz	Input mode supports up to fast-mode (400kb/s)
SHI Clock Duty Cycle	D_{SCK}	45	50	55	%	
SHI SDA Input Setup Time	t_{DS}	10	-	-	Ns	
SHI SDA Input Hold Time	t_{DH}	10	-	-	Ns	

* Power-off to power-down waiting time depends on the power supply discharge time in the system. Larger power supply decoupling capacitors in the system may take longer time to discharge. The discharging component may help shortening the time.
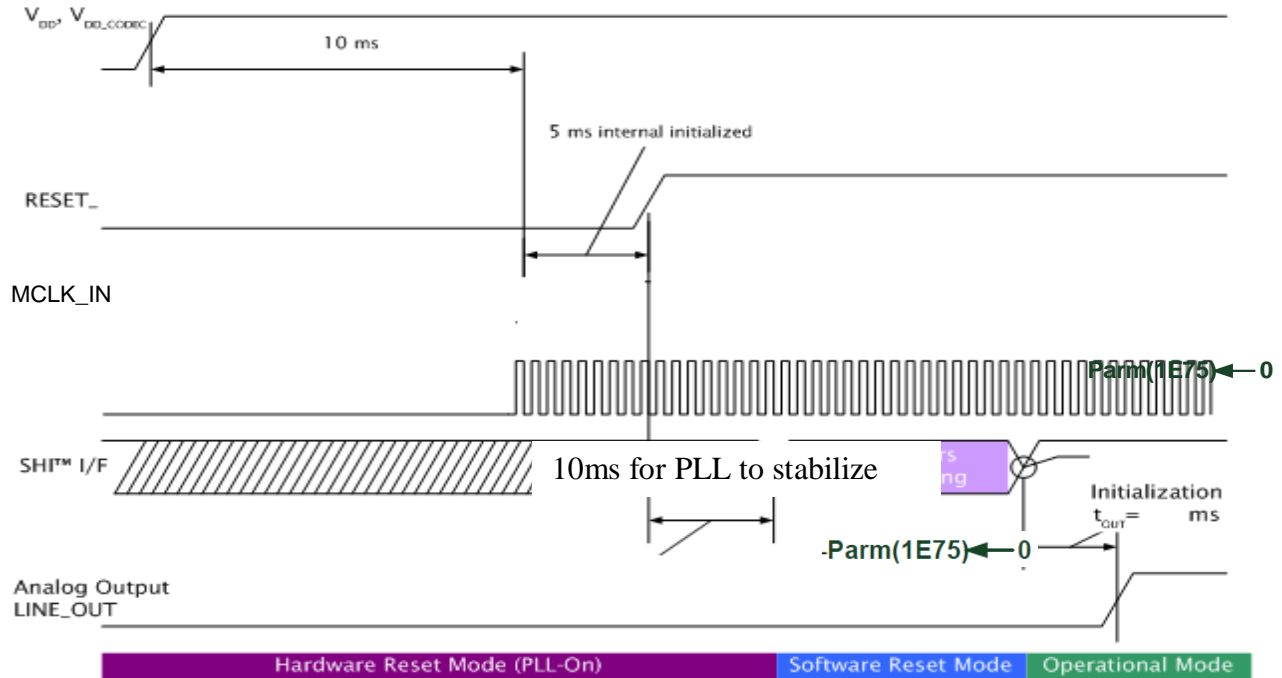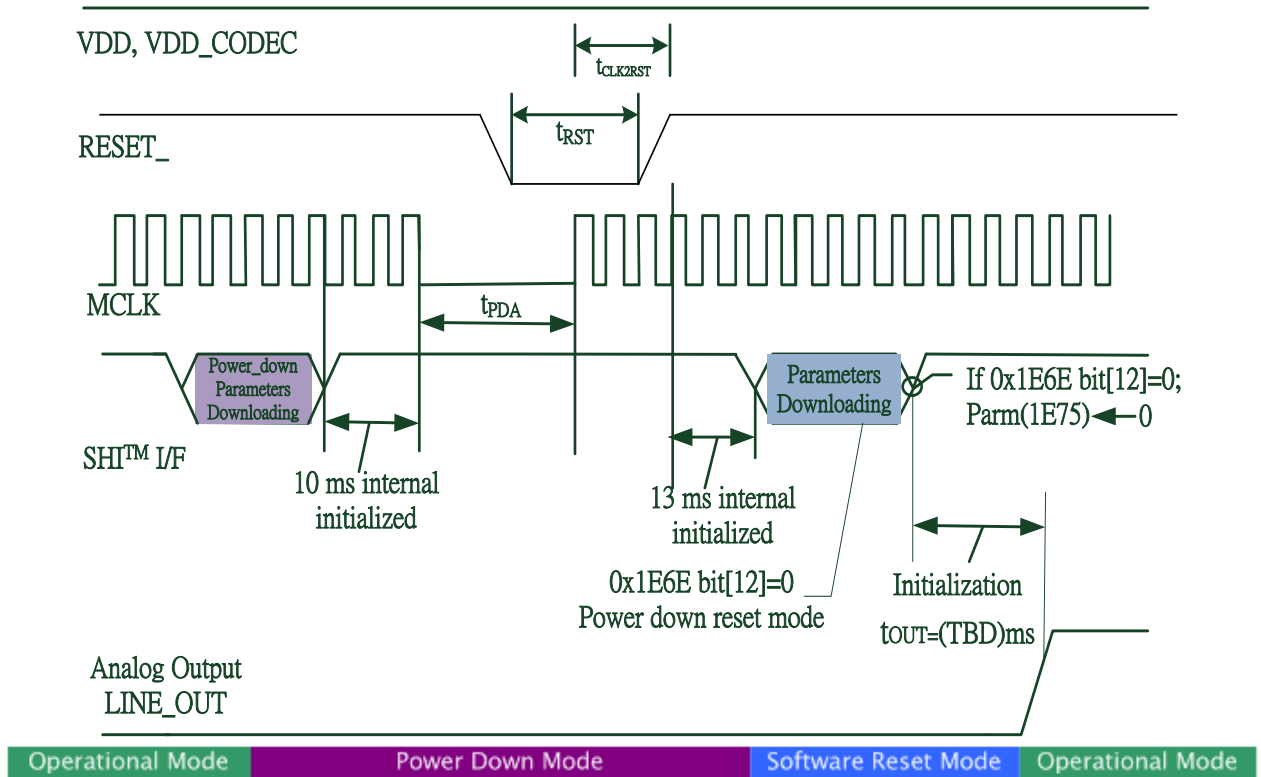
Figure 10: Cold Reset Timing Chart

Note: All input pins should be kept low (at GND) level before the chip (VDD) is powered. Failure to ensure the logic state of inputs before power supply settles, may cause malfunction of the processor.
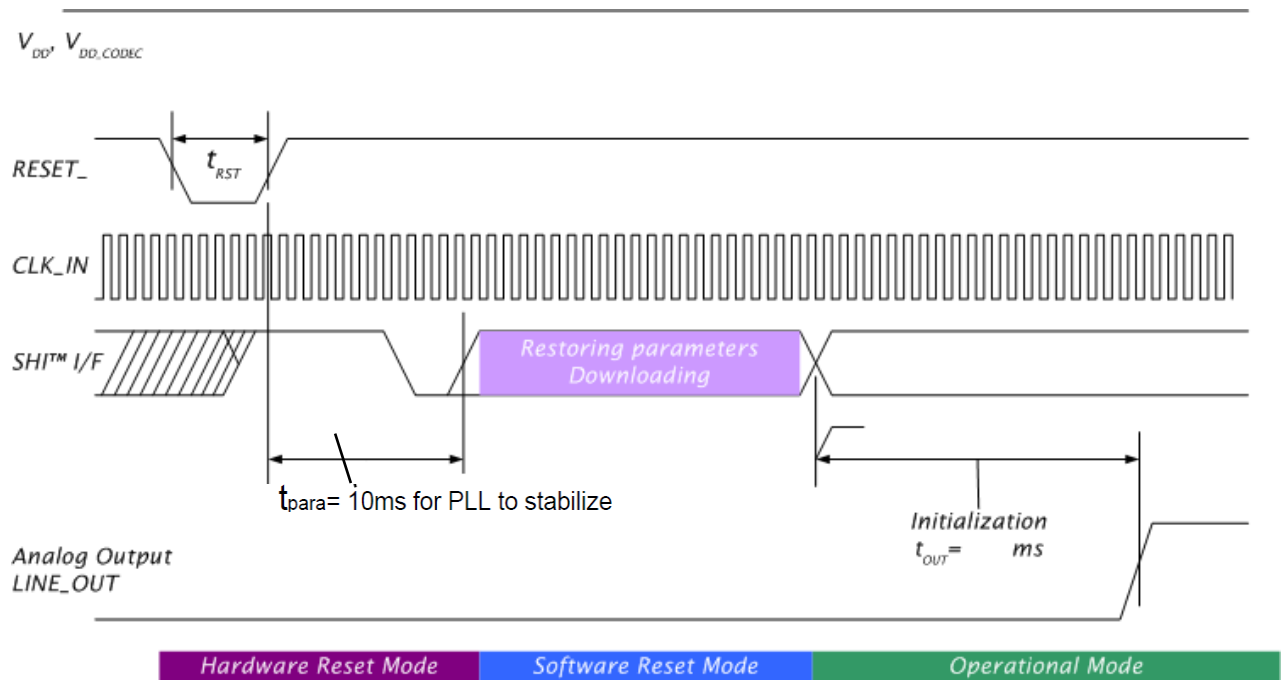
Figure 11: External Hardware Power Reset Timing Chart

Figure 12: External Power-Down Timing Chart

# 4. Pin Definition Details

Table 8: WLCSP Pin Description

Pin number	Pin name	type	Description
A1	Reserved		
A2	Reserved		
A3	MIC1_P	Analog In	Microphone 1 input (+).
A4	MIC0_P	Analog In	Microphone 0 input (+).
A5	MIC0_N	Analog In	Microphone 0 input (-).
B1	SDA	Digital In/Out	This pin is a serial data input/output of I2Cwith 3.3V tolerance.
B2	RST_	Digital In	Reset input. Active low. This pin is 3.3V tolerant.
B3	MIC1_N	Analog In	Microphone 1 input (-).
B4	LINE_IN_N	Analog In	Line-in input (-).
B5	LINE_IN_P	Analog In	Line-in input (+).
C1	VSS	GND	Digital ground.
C2	SCLK	Digital In	Clock input of I2C. This pin is a slave clock input with 3.3V tolerant. And it can speed up to 400kb/s with a proper pull-up resistor.
C3	VSSA	GND	Analog ground
C4	LINE_OUT_P	Analog Out	Line-out output (+).
C5	LINE_OUT_N	Analog Out	Line-out output (-).
D1	MCLK	Digital In	Master clock input.
D2	VDD	Power	Digital Power Supply
D3	GPIO0	Digital In/Out	GPIO pin
D4	VDDA	Power	Analog Power Supply
D5	VREF	Power Output	Reference Voltage Output Pin. About 0.5 PVDDA.

Note:
    IN – input pin
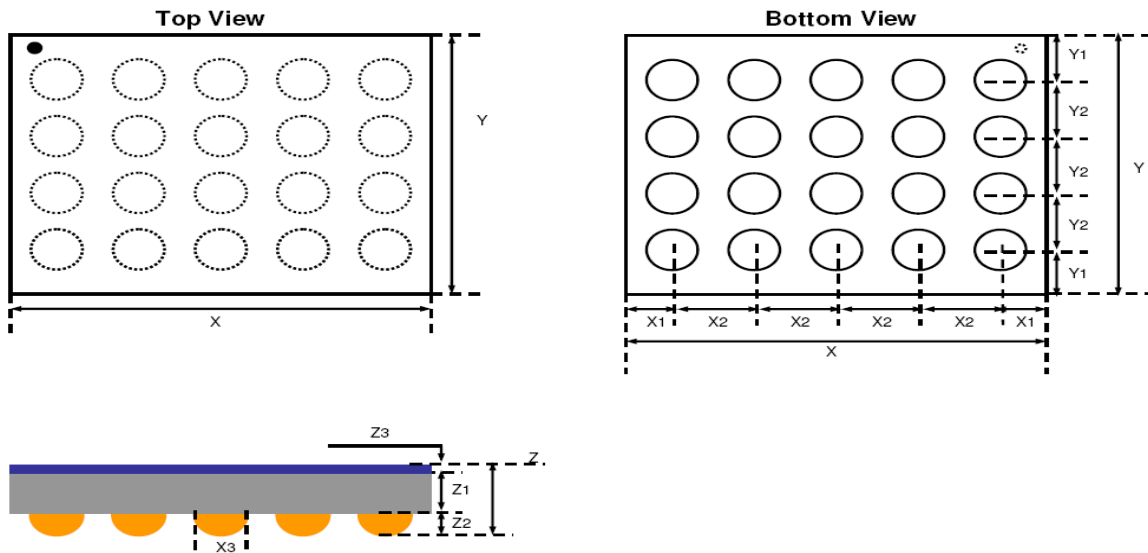   OUT – Output pin
    IN/OUT – Input/Output bidirectional pin

5. Package Dimensions

FM23-CE-382B Top, Bottom, and Side View

W: CSP
C : CSP with backside coating

E: Extended Grade

Trace code

0.10
0.12
0.54
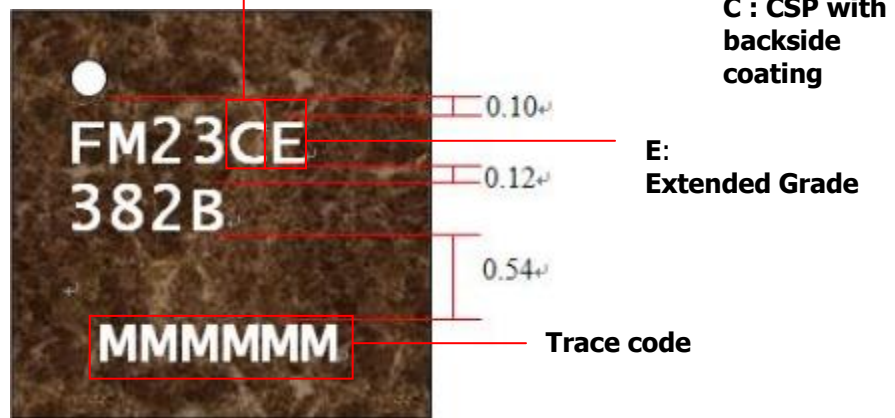
Font size tolerance: (+/- 0.05mm)

Marking shift tolerance: (+/-0.15mm)

Description	Symbol	Unit	Dimension
IC Length	X	um	2646.4+/-10
IC Width	Y	um	2213.5+/-10
Space between edge and pad center	X1	um	323.2+/-10
Space between adjacent pad	X2	um	500
Bump Diameter	X3	um	260+/-25
Space between edge and pad center	Y1	um	356.7+/-10
Space between adjacent pad	Y2	um	500
Height IC+Bump+Backside Coating	Z	um	798+/-30
Height IC	Z1	um	573
Bump	Z2	um	200+/-20
Backside Coating	Z3	um	25+/-10

Figure 13: CSP Package Dimensions

6. Ordering Infomation

Table 9: Available Package Type and Temperature Range

Order Code	FM23-CE-382B
Package Type	Proprietary 20-pin WLCSP Package with back side coating(0.04mm±0.004)
Package Size and Dimensions	2.646±0.01mm(L) × 2.213±0.01mm(W) × 0.798±0.03mm(H)
Pitch	0.5 mm
Lead-free	Green
Temperature Range Grade	Extended Grade
ESD Protection	HBM 2 kV/MM 200V
Operational Temperature Range (T_{amb})	Extended Grade, -20°C to 70 °C
Storage Temperature Range (T_{stg})	-40°C to 150°C

Reference

Terminology

Table 10: Terminology

Term	Definition
AEC	Acoustic Echo Cancellation
BF	Beam-Forming
ADC	Analog to Digital Conversion
DAC	Digital to Analog Conversion
DRC	Dynamic Range Control
ESD	ElectroStatic Discharge
GPIO	General Purpose Input/Output
LO	Line out
MIC	Microphone
PCM	Pulse Code Modulation
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
RAM	Random Access Memory
ROM	Random Only Memory
SOC	System on Chip
SHI	Serial Host Interface
SNR	Signal to Noise Ratio
WLCSP	Wafer Level Chip Scale Integration

Related References

Table 11: Document References

Document	Location
FM-23 Product Brief	Fortemedia sales and support
FM-23 Schematics Layout Guide	Fortemedia sales and support
FM-23 Reference Design Schematics	Fortemedia sales and support
FM WLCSP Voice Processors – PCB Design and Assembly Guide	Fortemedia sales and support
FM-23 Configuration Manual	Fortemedia sales and support
FM-23 Evaluation Module – Operational Manual	Fortemedia sales and support