G1N65R240PB

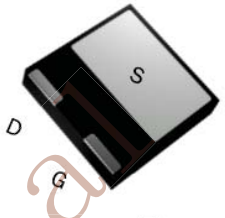
650V GaN FET

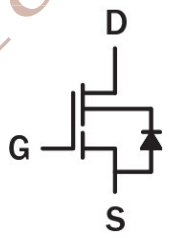
Preliminary Datasheet

1. Description

The G1N65 series FETs are hybrid normally-off Gallium Nitride (GaN) field effect transistors with the strongest gate and the lowest reverse voltage drop of all wide-band-gap devices in the market. They allow simple gate drive, offer best-in-class performance and outstanding reliability.

8x8 PQFN
(bottom view)





Schematic Symbol

Features

- Strong gate with a high threshold, no need for negative gate drive, and a high repetitive input voltage tolerance of ±18V.
- Fast turn-on/off speed for reduced cross-over losses.
- Low Q_G and simple gate drive for lowest driver consumption at high frequencies.
- Lowest V_F in off-state reverse conduction among all SiC and GaN FETs for low loss during dead-times.
- Low Q_{RR} for outstanding hard-switched bridge applications.
- High spike tolerance of 800V for enhanced reliability.

Benefits

- Enable highest conversion efficiencies.
- Enable higher frequency for compact power supplies.
- End-product cost & size savings due to reduced thermal budget.
- Improved safety & reliability due to cooler operation temperature.

Applications

- High-frequency compact chargers with QR or ACF flyback topologies.
- Half-bridge buck/boost, totem-pole PFC circuits or inverter circuits.
- High-efficiency/ High-frequency LLC or other soft-switching topologies.

Key Performance Parameters	
V_{DSS} (V)	650
$V_{DS(PK)}$ (V) [a]	800
$R_{DS(ON)}$ (mΩ) typical [b]	240
Q_{OSS} (nC)	19
Q_G (nC)	8

[a] Duty<1%, spike duration <1μs, nonrepetitive
[b] Dynamic on-resistance

Part Number & Package Information		
Part #	Package	Package Base
G1N65R240PB	PQFN 8x8 (mm)	Source

2. Maximum Ratings & Thermal Characteristics

Name	Parameter	Value
V_{DSS} (V)	Maximum drain-to-source voltage (T_j = -55°C to 150°C)	650
$V_{DSS(PK)}$ (V)	Maximum peak drain-to-source voltage [a]	800
V_{GSS}(V)	Maximum gate-to-source voltage	±18
P_D(W)	Maximum power dissipation (T_C=25°C)	21
I_{DS}(A)	Maximum continuous drain current (T_C=25°C)	6.5
	Maximum continuous drain current (T_C=100°C)	4
I_{DS}(Pulsed)(A)	Maximum pulse drain current (T_C=25°C) [b]	30
T_c (°C)	Case temperature	-55 to +150
T_j (°C)	Junction temperature	-55 to +150
T_s (°C)	Storage temperature	-55 to +150
$R_{\Theta JC}$ (°C/W)	Junction-to-case thermal resistance	5.5
$R_{\Theta JA}$ (°C/W)	Junction-to-ambient thermal resistance [c]	50
T_{sold} (°C)	Reflow soldering temperature [d]	260

[a] Duty cycle<1%, spike duration <1μs

[b] Pulse width=10μs

[c] Soldered on a PCB of 6cm² metal area

[d] Reflow MSL3

3. Device Characteristics

T_j=25℃ unless specified

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DSS}	Drain-to-source voltage	650	-	-	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	1.6	2.1	2.6	V	V_{DS}=V_{GS}, I_D=0.5mA
$R_{DS(ON)}$	Drain-source on resistance [a]	-	240	300	mΩ	V_{GS}=8V, I_D=5A
		-	492	-	mΩ	V_{GS}=8V, I_D=5A, T_j=150°C
I_{DSS}	Off-state drain-to-source leakage current	-	1.2	12	μA	V_{DS}=650V, V_{GS}=0V
		-	8	-	μA	V_{DS}=650V, V_{GS}=0V, T_j=150°C
I_{GSS}	Gate-to-source leakage current	-	-	100	nA	V_{GS}=18V
		-	-	-100	nA	V_{GS}=-18V
C_{ISS}	Input capacitance	-	760	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
C_{OSS}	Output capacitance	-	16	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
C_{RSS}	Reverse switching capacitance	-	2	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
$C_{O(ER)}$	Equivalent output capacitance (energy related)	-	24	-	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(TR)}$	Equivalent output capacitance (time related)	-	47	-	pF	V_{GS}=0V, V_{DS}=0V to 400V
Q_G	Total gate charge	-	8	-	nC	V_{DS}=400V, V_{GS}=0V to 8V, I_D=4A
Q_{OSS}	Output charge	-	19	-	nC	V_{GS}=0V, V_{DS}=0V to 400V
$t_{D(ON)}$	Turn on delay time	-	19	-	ns	V_{DS}=400V, V_{GS}=0V to 8V, I_D=4A, R_G=30Ω
t_R	Rise time	-	3.4	-	ns	
$t_{D(OFF)}$	Turn off delay time	-	53	-	ns	
t_F	Fall time	-	10	-	ns	

[a] Dynamic ON-resistance

Reverse Device Characteristics, T_j=25℃ unless specified

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
I_S	Reverse current	-	-	4	A	V_{GS}=0V, T_C=100°C, ≤25% duty cycle
V_{SD}	Reverse voltage [a]	-	1.5	-	V	V_{GS}=0V, I_S=4A
t_{RR}	Reverse recovery time	-	16	-	ns	I_S=4A, V_{DD}=400V, di/dt=1000A/μs
Q_{RR} [b]	Reverse recovery charge	-	23	-	nC	I_S=4A, V_{DD}=400V, di/dt=1000A/μs

[a] Including the effect of Dynamic ON-resistance

[b] Including C_{OSS}

4. Typical Characteristics (T_C=25 ℃ unless specified)

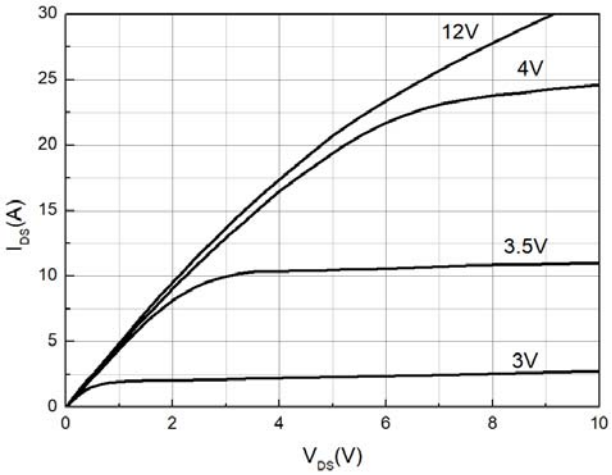


Figure 1. Typical Output Characteristics at T_j=25 ℃ (Parameter: V_{GS})

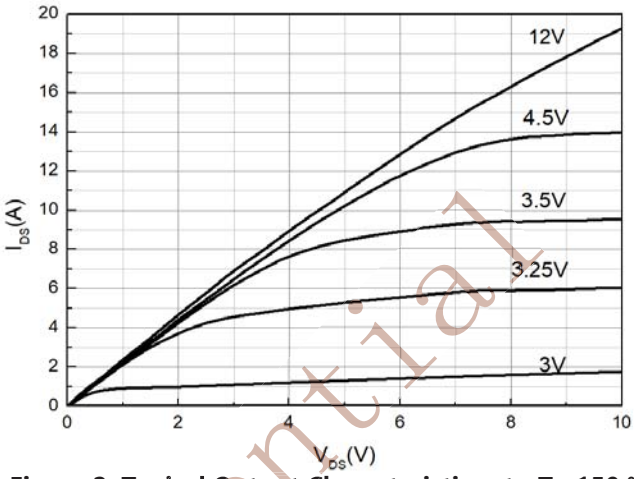


Figure 2. Typical Output Characteristics at T_j=150 ℃ (Parameter: V_{GS})

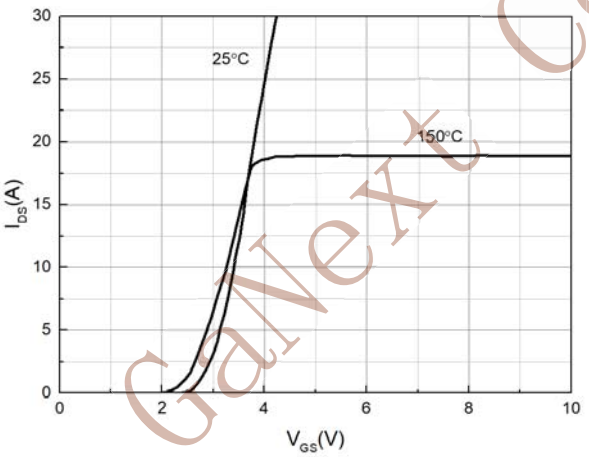


Figure 3. Typical Transfer Characteristics (V_{DS}=10V, parameter: T_j)

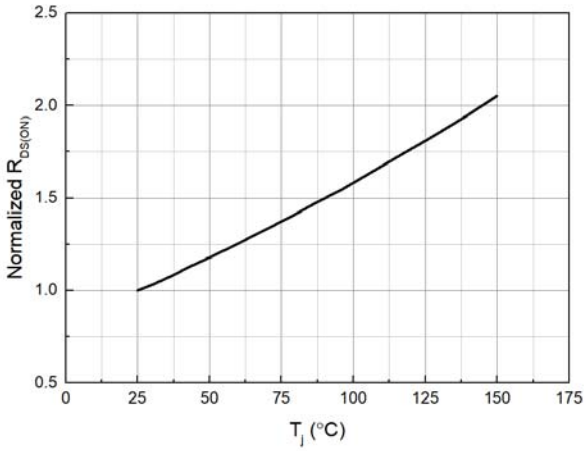


Figure 4. Normalized On-resistance (I_D=5A, V_{GS}=8V)

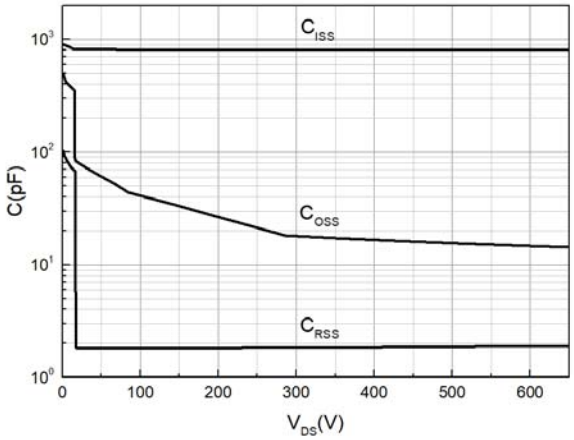


Figure 5. Typical Capacitance
(V_{GS}=0V, f=1MHz)

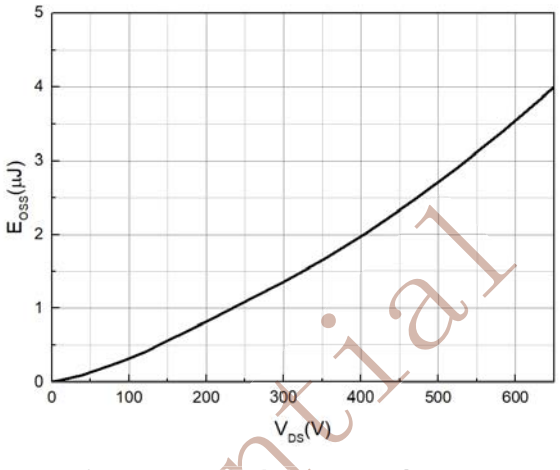


Figure 6. Typical C_{OSS} Stored Energy

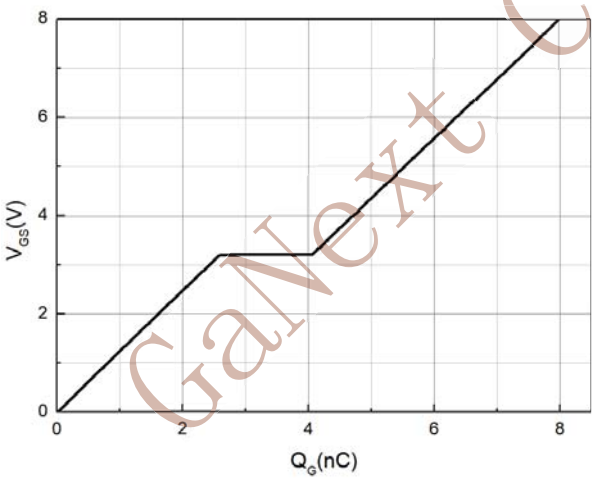


Figure 7. Typical Gate Charge
(I_{DS}=4A, V_{DS}=400V)

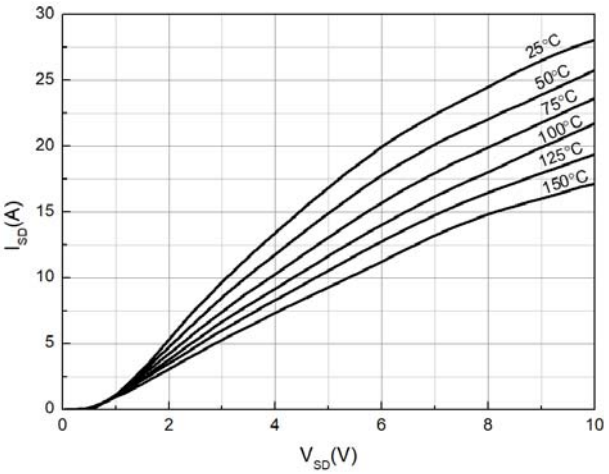


Figure 8. Reverse Conduction Characteristics
(Parameter: T_j)

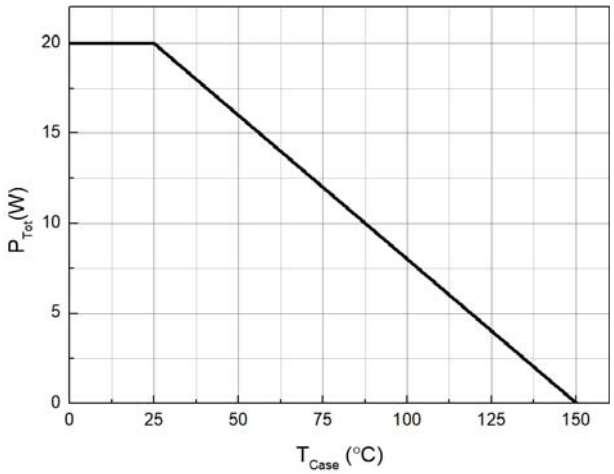


Figure 9. Power Dissipation

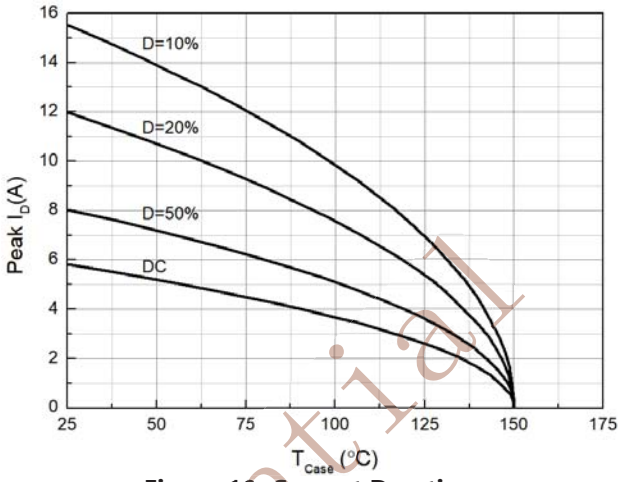


Figure 10. Current Derating
(Pulse width：10μs, V_{GS}：8V)

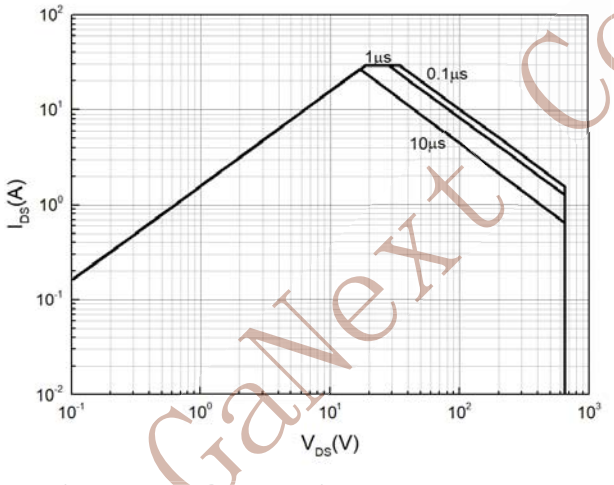


Figure 11. Safe Operating Area at T_C=25°C

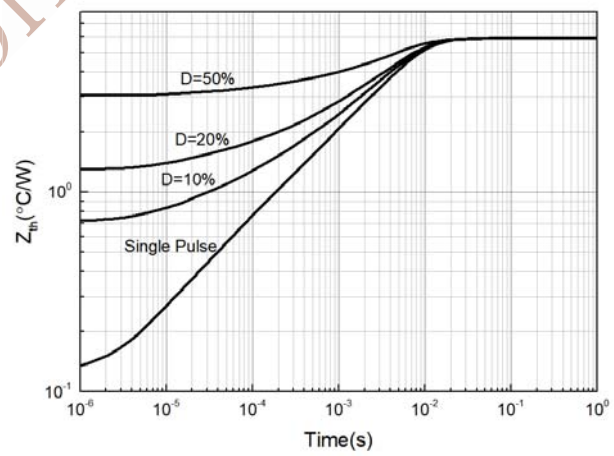


Figure 12. Transient Thermal Resistance

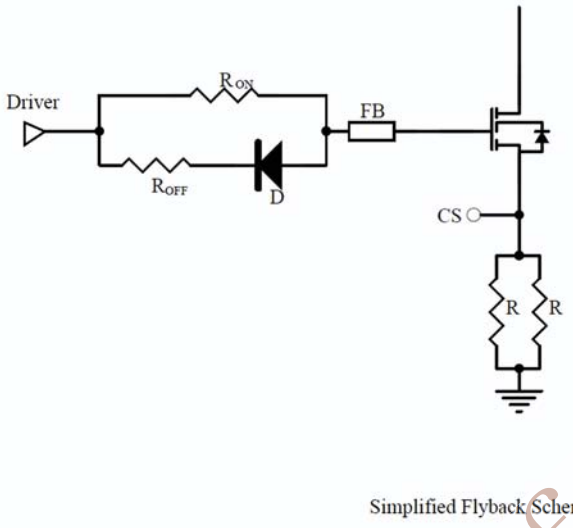
5. Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

DO	DO NOT
Place gate drives close to the GaN device and separate input traces from output traces	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long gate drive traces, long lead length and route the output traces next to the input
Use gate ferrite bead and dc-link RC snubber	Use close-by decoupling capacitor without series resistor

6. Circuit Implementation

(1) Simplified flyback schematic:

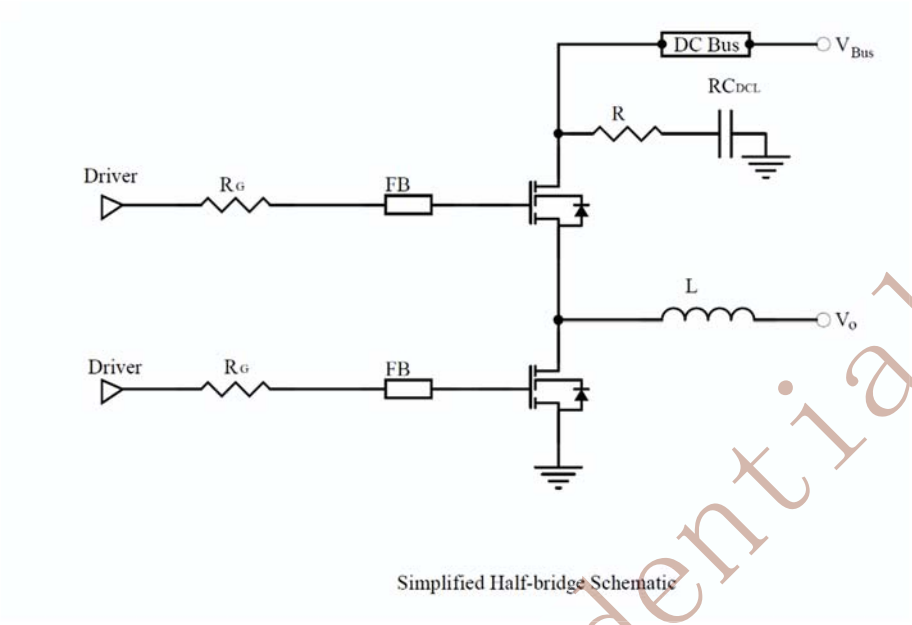


Simplified Flyback Schematic

Recommended gate drive: (0V, 12V)

Ferrite Bead (FB)	R_{ON}	R_{OFF}
200-300Ω at 100MHz	100-300Ω	2-10Ω

(2) Simplified half-bridge schematic:



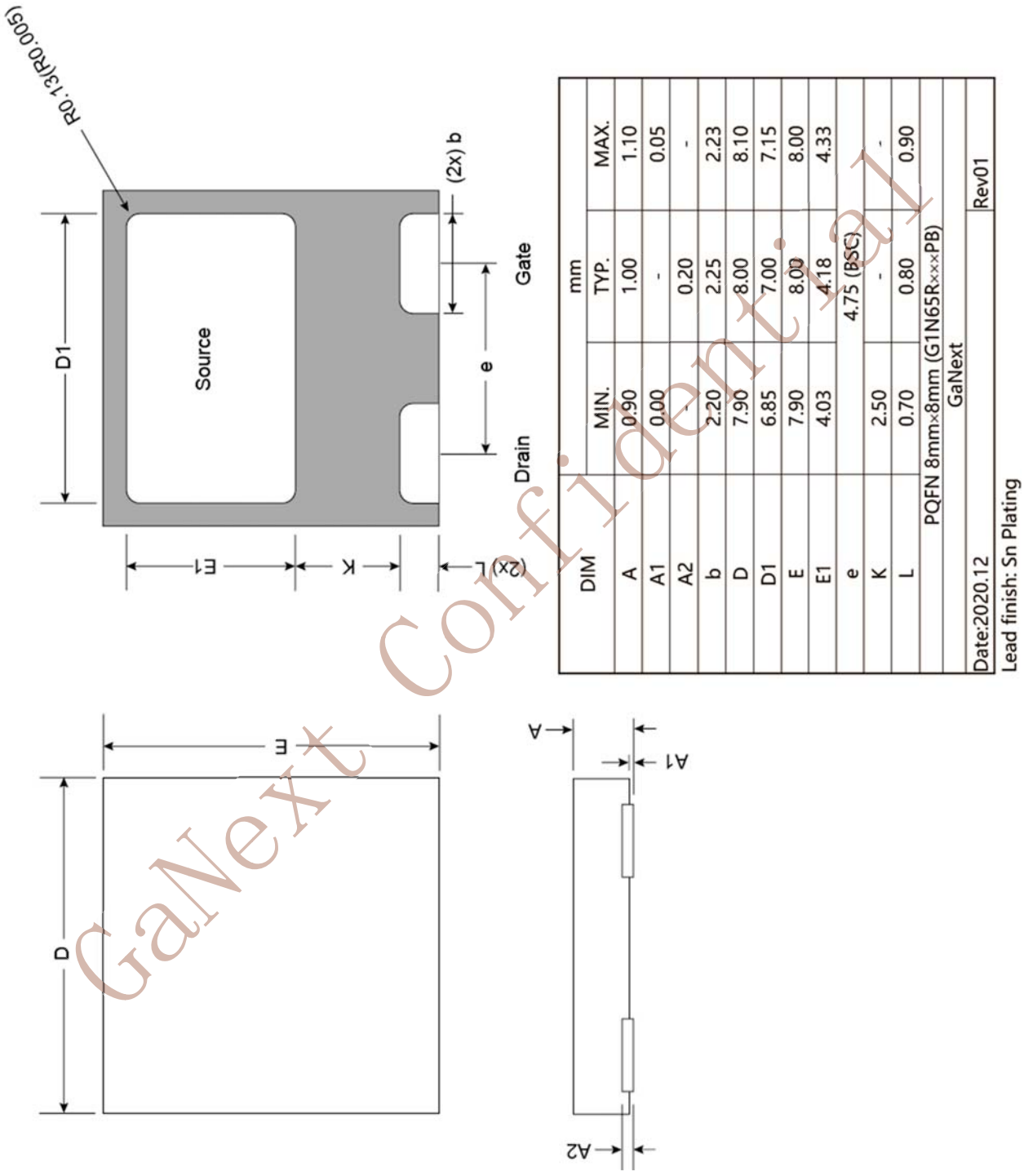
Simplified Half-bridge Schematic

Recommended gate drive: (0V, 1V) with $R_{G(tot)}$ = 30 Ω [a)]

Gate Ferrite Bead (FB)	Required DC Link RC Snubber (RC_{DCL}) [b)]
200-300Ω@100MHz	4.7-10nF + 5Ω

Notes:
[a)] For bridge topologies only. R_G could be smaller in single ended topologies.
[b)] RC_{DCL} should be placed as close as possible to the drain pin. Other decoupling capacitors should be located away from the RC_{DCL}.

7. Package Dimensions



DIM	mm MIN.	TYP.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A2	-	0.20	-
b	2.20	2.25	2.23
D	7.90	8.00	8.10
D1	6.85	7.00	7.15
E	7.90	8.00	8.00
E1	4.03	4.18	4.33
e		4.75 (BSC)	
K	2.50	-	-
L	0.70	0.80	0.90

PQFN 8mm×8mm (G1N65R×××PB)
GaNext
Date:2020.12 Rev01
Lead finish: Sn Plating

8. Revision History

Revision No.	Date	Description of Change(s)
Rev01	2020-12-15	Release of final version
Rev02	2021-02-07	Update datasheet